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TO ALL WHOM IT MAY CONCERN:

Be it known that WE, AXEL BRINTZINGER and INGO UHLENDORF, citizens of Germany, whose post office addresses are Louisenstrasse 70, D-01099, Dresden, Germany, and Boehmische Strasse 13, D-01099, Dresden, Germany, respectively, have made an invention in a

METHOD FOR THE SOLDER-STOP STRUCTURING OF ELEVATIONS ON WAFERS

of which the following is a

SPECIFICATION

BACKGROUND OF THE INVENTION

[0001] The increasing integration of semiconductor components, the increasing number of necessary electrical connections between semiconductor chips and carrier elements and, in particular, the requisite miniaturization with the aim of the flattest possible subassemblies, have led to the practice of making direct contact between semiconductor chips and carrier elements, e.g., flip-chip bonding. This practice has led to a considerable simplification of semiconductoir mounting technology, since metallic intermediate carriers and the production of wire links are no longer required in order to make electrical contact.

[0002] However, in order to make possible the direct contact between semiconductor chips and carrier elements such as printed circuit boards ("PCBs"), it is necessary to produce 3D structures,

known as bumps or soldering mounds, on the semiconductor chip, which at their respective highest point have a gold-plated contact surface and are connected via a conductor track to a bonding pad of the wafer. These gold-plated contact surfaces can then be provided with a micro ball or the like of a solder material and connected electrically and mechanically to a corresponding soldering contact on the PCB.

[0003] In order to achieve a certain equalization of mechanical loadings on the completed subassemblies, for example caused by different thermal coefficients of expansion of the individual components or caused during their handling, the basic structure of the bumps is produced from a compliant material, e.g., silicone, so that a three-dimensional, mechanically flexible structure is produced.

[0004] The conductor tracks used for the electrical connection between the bonding pads and the bumps consist, for example, of a seed layer, on which a Cu conductor track and, above the Cu conductor track, a Ni layer are grown, the latter being used to protect the Cu layer against corrosion. A dielectric is used underneath the seed layer and the bumps to ensure that there is an electrical connection only between the gold-plated contact surface on the bump and the associated bonding pad.

[0005] In order to achieve solderability, the nickel layer must be coated with gold at the appropriate points, i.e., the tips of the three-dimensional ("3D") structures.

[0006] In the process, it is absolutely necessary to ensure that the gold coating is applied only to the tips of the 3D structures and that the redistribution layer, which leads down from the 3D structures, is absolutely free of gold. This creates a solder stop when the semiconductor chip is soldered onto a carrier element. Without this solder stop, the solder material would flow in an

uncontrolled manner over the redistribution layer and have a detrimental effect on mechanical and electrical properties which could negatively impact the reliability of the finished electronic subassembly.

[0007] In the method commonly used in present manufcaturing processes, the necessary structuring of the gold layer is implemented by means of a generally known lithographic process. In this method, immediately after the seed layer and the Cu/Ni layer of the redistribution layer are applied, the gold is deposited on the entire redistribution layer. The gold layer is then covered by lithography in such a way that selective etching or stripping of the undesired gold layer can be performed. Upon completion of this method, a gold layer remains only immediately on the tip of the 3D structure.

[0008] In further detail, this currently-used method is performed using the following steps. First, the deposition of the seed layer is performed. Next, an EPR1 (epoxy photoresist 1) coating and structuring is applied during the first lithography step. Next, the reroute plating, production of the Cu/Ni layer on the seed layer is completed. The reroute trace is then coated with Au. Next, EPR2 (epoxy photoresist 2) coating and structuring is performed as a second lithography step. Finally, the Au layer is selectively etched using wet etching or removal/stripping techniques.

[0009] The result of this process is a 3D structure with a gold coating on its tip. However, the side flanks of the structure remain unprotected. While this may ensure that, during the subsequent connection of the wafer to a PCB, no solder material can flow away laterally over the flanks of the 3D structure (which could lead to functional disruption), the Ni layer is likewise exposed during the Au etching/stripping is accordingly completely unprotected against corrosion. This is a significant disadvantage of this known method.

[0010] In another method which is commonly used in practice, the 3D structures are initially connected to the associated bonding pad as already described with conductor tracks of Au-coated Cu/Ni layers and are subsequently embedded in a potting compound in such a way that only the tips of the 3D structures remain free. However, this method is difficult to perform properly and can be inefficient.

SUMMARY OF THE INVENTION

[0011] In a method according to the present invention, the solder-stop structuring of elevations on wafers which can be performed reliably while ensuring good flank protection of the 3D structure.

[0012] In one embodiment of a method in accordance with the present invention, a metallization layer is coated with an Au layer. Next, resist is deposited in a selected local solder area on the tip of a 3D contact structure Then a solder stop layer is deposited over the 3D contact structure, including the resist. Finally, the resist on the tip of the 3D structure is removed, including the solder stop layer covering said resist.

[0013] The present invention thereby provides a reliable method for solder-stop structuring of 3D structures. At the same time, effective flank protection of the Ni surface of the 3D structures is achieved. Corrosion of the Cu layer and of the Ni layer are prevented effectively, and the reliability of electronic subassemblies produced by this method is substantially improved.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] For a more complete understanding of the present invention, the needs satisfied thereby, and the objects, features, and advantages thereof, reference now is made to the following descriptions taken in connection with the accompanying drawings:

[0015] Figure 1 shows a wafer with a 3D structure made of a compliant element following the deposition of the seed layer and the deposition of a photoresist EPR1;

[0016] Figure 2 shows the 3D structure according to Figure 1 after the coating with the Cu/Ni layer;

[0017] Figure 3 shows the 3D structure according to Figure 2 after the coating with a Au layer within the limitation by EPR1;

[0018] Figure 4 shows the 3D structure after the etching of the seed layer and the coating with a resist on its tip or upper surface;

[0019] Figure 5 shows the 3D structure after coating with a solder stop layer; and

[0020] Figure 6 shows the 3D structure after the thermal removal of the resist by means of a lift-off process.

DETAILED DESCRIPTION OF THE INVENTION

[0021] Figures 1 through 6 show the method of producing a 3D structure 1 comprising a compliant element 2 on a wafer 3 with simultaneous solder-stop structuring. The finished 3D

structure 1 is illustrated in Figure 6. The structure comprises a seed layer 4, which has been deposited on the wafer 3 and enclosing the compliant element 2. Above the seed layer is a Cu layer 5 is deposited and, above that, a Ni layer 6 (Figure 2).

[0022] The Ni layer 6 is covered by a thin solderable Au layer 7, which also extends laterally over the flanks of the 3D structure 1. The flanks of the 3D structure 1 and adjacent regions of the 3D structure 1 are covered with a solder stop layer 8 to ensure that, during a soldering operation, no solder material can flow down laterally from the 3D structure 1. This solder stop layer 8 leaves only the upper region of the Au layer 7 exposed, so that a subsequent soldering operation can extend only over the exposed surface of the Au layer 7. The solder stop layer 8 can also project slightly beyond the surface of the Au layer 7 forming a rim 9.

[0023] This 3D structure 1 is produced in accordance with the process flow which is described hereinafter. First, deposition of the seed layer 4 is performed on the wafer 3 and the compliant element. Next, a photoresist and structuring are applied to form an EPR1 mask 10. The resist used is preferably an epoxy photoresist which may be removed thermally by means of a lift-off step. Then a reroute plating step is performed by applying a Cu layer 5 and Ni layer 6. A final coating of Au layer 7 is applied. Next, the EPR1 mask 10 is removed and the exposed surfaces of the seed layer 4 are etched. Then the deposition and structuring of a resust 11 on the top surface of the Au layer is performed. The entire 3D structure 1 is then coated with the solder stop layer 8. Finally, the resist 11 and the solder stop material covering the resist are removed by means of a thermal lift-off process so that the Au layer 7 on the tip of the 3D structure 1 is exposed.

[0024] This method describes the production of a complete 3D structure 1. A description of the production of the conductor tracks between the 3D structure and associated bonding pad has been omitted since this is well-described in the art and can be performed using known methods.

[0025] In a further embodiment of the present invention, the solder stop layer may be deposited at least in the region of the 3D structure.

[0026] Furthermore, the layer structure of the conductor track is built up on a seed layer, which also encloses the resilient or compliant contact bump, by which means a metallization which adheres firmly can be produced.

[0027] In yet another exemplary embodiment of the present invention, the solder stop layer may consist of a mineral material such as boron nitride such that, during the thermal removal of the EPR or of another suitable resist, the solder stop layer on the EPR is also removed.

[0028] In another exemplary embodiment of the present invention, the Cu/Ni layers of the conductor track are deposited within the EPR1 mask and the EPR1 mask is then removed, the solder stop layer then being deposited.

[0029] While there have been described various embodiments of the invention, those skilled in the art will recognize that other changes and modifications may be made thereto without departing from the spirit of the invention, and it is intended to claim all such changes and modifications as fall within the true scope of the invention.